WHAT IS CLAIMED IS:

1. A method for managing power consumption in a computer system having a processor, comprising the steps of:

providing an array of redundant power supplies, wherein each power supply in the array is rated to a power delivery capacity that is less than the maximum power draw of the computer system;

identifying the loss of operation of a power supply of the redundant power supply array; and

reducing the operating speed of the processor of the computer system.

2. The method for managing power consumption in a computer system of claim 1, wherein the step of reducing the operating speed of the processor of the computer system comprises the step of asserting a signal to an input of the processor to cause the processor enter a power management mode.

3. The method for managing power consumption in a computer system of claim 1, wherein the step of reducing the operating speed of the processor of the computer system comprises the step of asserting a signal to an input of the processor to cause the processor to turn a clock off the processor on and off successively.

4. The method for managing power consumption in a computer system of claim 1, wherein the step of identifying the loss of operation of a power supply of the redundant power supply array comprises the step of notifying the BIOS of the computer system of the loss of operation of a power supply of the redundant power supply array.

5. The method for managing power consumption in a computer system of claim 4, wherein the signal at the processor is asserted by the BIOS of the computer system.

6. The method for managing power consumption in a computer system of claim 1, further comprising the step of increasing the operating speed of the processor in conjunction with the operation of all power supplies of the redundant power supply array.

7. A computer system, comprising:

an array of redundant power supplies, wherein each power supply of the array is rated to a power delivery capacity that is less than the maximum power draw of the computer system; and

a processor;

wherein the operating speed of the processor is reduced upon the loss of a power supply of the array of redundant power supply whereby the power draw of the computer system is reduced to a level below the rated capacity of the functioning power supplies of the array.

8. The computer system of claim 7, wherein the operating speed of the processor is reduced by the assertion of a signal at the processor to cause the processor to enter a system management mode.

9. The computer system of claim 7, wherein the operating speed of the processor is reduced by turning a clock of the processor on and off successively.

10. The computer system of claim 7, wherein the array of redundant power supplies includes an array controller for identifying the failure or removal of a power supply of the array.

11. The computer system of claim 7, further comprising a BIOS for receiving an indication of a loss of a power supply and for asserting a signal to cause the processor to reduce the clock speed of a clock in the processor.

12. The computer system of claim 11, wherein the operating speed of the processor is reduced by turning a clock of the processor on and off successively.

13. The computer system of claim 7, further comprising a BIOS for receiving an indication of a loss of a power supply and for asserting a signal to cause a lower voltage level to be applied to the processor.

14. The computer system of claim 7, further comprising a BIOS for receiving an indication of a loss of a power supply and for asserting a signal to reduce the data rate of the front side bus of the processor.

15. A method for conserving power in a computer system having multiple processors and an array of redundant power supplies, comprising the steps of:

identifying the loss of operation of a power supply of the redundant power supply array;

identifying the processor having the highest operating speed;

reducing the operating speed of the processor having the highest operating speed.

16. The method for conserving power in a computer system of claim 15, wherein the step of reducing the operating speed of the processor having the highest operating speed comprises the step of asserting a signal to an input of the processor to cause the processor enter a power management mode.

17. The method for conserving power in a computer system of claim 15, wherein the step of reducing the operating speed of the processor having the highest operating speed comprises the step of asserting a signal to an input of the processor to cause the processor to turn a clock off the processor on and off successively.

18. The method for conserving power in a computer system of claim 15, further comprising the step of increasing the operating speed of the processor having the highest operating speed in conjunction with the operation of all power supplies of the redundant power supply array.

19. The method for conserving power in a computer system of claim 15, wherein each power supply of the redundant power supply array is rated to a power delivery capacity that is less than the maximum power draw of the computer system.

20. A method for reducing the power draw of a computer system having an array of redundant power supplies, wherein each power supply is rated to a power delivery capacity that is less than the maximum power draw of the computer system, comprising the steps of:

identifying the loss of a power supply of the computer system;

determining whether the power draw of the computer system has reached or exceeds a predetermined threshold level; and

causing the processor to enter a power conservation state when the power draw of the computer system reaches or exceeds the threshold level.

21. The method for reducing the power draw of a computer system of claim 20, wherein the step of causing the processor to enter a power conservation state comprises the step of causing the processor to reduce the effective rate of at least one internal clock of the processor.

22. The method for reducing the power draw of a computer system of claim 21, wherein the step of causing the processor to enter a power conservation state comprises the step reducing the effective rate of at least one internal clock of the processor to turn on and off according to a duty cycle.

23. The method for reducing the power draw of a computer system of claim 20, wherein the step of causing the processor to enter a power conservation state comprises the step of causing a lower voltage level to be applied to the processor.

24. The method for reducing the power draw of a computer system of claim 20, wherein the step of causing the processor to enter a power conservation state comprises the step of lowering the data rate of the front side bus of the processor.